4/4 B.Tech. EIGHTH SEMESTER
ELECTIVE – IV

EM8T3B LOW POWER VLSI DESIGN Credits: 3

Lecture: 3 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course Objective

To study the concepts on different levels of power estimation and optimization techniques.

Learning Outcome:

To design chips used for battery-powered systems and high-performance circuits not exceeding power limits.

UNIT I
Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

UNIT II
Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

UNIT III
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

UNIT IV
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques,signal entropy. Low Power Design

UNIT V
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

UNIT VI
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT VII
Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design**.**

UNIT VIII

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Reference Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
4. Low Power Design in Deep Sub-micron Electronics by W. Nebel and J. Mermet, Kluwer Academic Publishers, 1997
5. Gary K. Yeap, Practical Low power Digital VISI Design, Kluwer Academic Publishers, 1998.